APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/005,113	12/05/2001	Sandra Lynn Carrico	2001-0450	9439

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EXAMINER
CERVETTI, DAVID GARCIA

ART UNIT	PAPER NUMBER
2136	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

	Application No.	Applicant(s)
Office Action Summary	10/005,113	CARRICO ET AL.
	Examiner	Art Unit	
	David G. Cervetti	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _26 October 2006_.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-11_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-11_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _12 May 2005_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   Applicant's arguments filed October 26, 2006, have been fully considered but

they are not persuasive.

2.   Claims 1-11 are pending and have been examined.

Response to Amendment

3.   Regarding Applicant's argument that Sherer teaches only a single memory

module, Examiner respectfully submits that, one, the number of memory modules does

not determine patentability, since such alleged improvement to the system of Sherer

would have been obvious to someone of ordinary skill in the art, and two, Sherer does

explicitly show a program memory subdivided into multiple segments or modules (fig.

3). It is further submitted that Sherer teaches this feature, see col. 5lines 55-67 and col.

6, where the authentication is described, and how the information for authentication is

provided, using additional memory. **Applicant's arguments are not persuasive.**

4.   Regarding Applicant's argument that Examiner is using hindsight with respect to

the feature of erasing the information from the volatile memory at the completion of the

session, Examiner respectfully submits that such argument ignores the fact that at the

time the invention as made, one-time passwords were conventional and well known.

Sherer further discloses and/or suggests this feature in columns 5-6, where the

information used for authentication is provided/generated. **Applicant's arguments are**

not persuasive.

5.   *__The applicant has not adequately traversed the examiner's use of official__*

__notice with regards to the claimed limitation found in claim 5, this feature is taken__

__by the examiner to be admitted prior art since the applicant has not adequately__

__challenged the examiner's use of official notice (see MPEP 2144.03(c), 2144.04).__

Information Disclosure Statement

6.   It is noted that no Information Disclosure Statement has been filed on this

application.

Claim Rejections - 35 USC § 103

7.   The text of those sections of Title 35, U.S. Code not included in this action can

be found in a prior Office action.

8.   **Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over**

Sherer et al. (US Patent 6,115,376, hereinafter Sherer), and further in view of

Jones et al. (US Patent 5,623,637, hereinafter Jones).

Regarding claims 1 and 10, Sherer teaches a security mechanism for

enabling a user to commence a session between a network peripheral device and

a network **(column 5, lines 32-67)**, comprising:

-       an immutable memory element that contains first information including

        application software that initiates and provides security services **(column**

        5, lines 32-67);

-       a persistent memory element that contains second information to enable

        the security mechanism to configure the network peripheral device to

        access different networks **(column 5, lines 32-67)**;

-       a volatile memory element that contains third information, including

        the critical data for authentication **(column 5, lines 32-67)**.

Sherer does not expressly disclose third information erased from the volatile

memory at the completion of each connection session or a tamper-evident enclosure.

However, Sherer suggests using different authentication schemes **(column 5,**

lines 32-67), and Jones teaches a tamper-evident enclosure for enclosing the memory

elements **(column 2, lines 1-67, column 3, lines 1-67)**. Therefore, it would have been

obvious to one having ordinary skill in the art at the time the invention was made to use

session keys which are valid for just a session and deleted afterwards. One of ordinary

skill in the art would have been motivated to perform such a modification to use session

specific credentials and to provide means to detect attempted tampering **(Sherer,**

column 7, Jones, column 2).

Regarding claims 2 and 11, the combination of Sherer and Jones teaches

wherein the security services include authentication of the security mechanism itself and

authentication of the user to the network upon receipt of identification Information from

the security mechanism and the user, respectively **(Sherer, column 7, lines 1-67)**.

Regarding claim 3, the combination of Sherer and Jones teaches wherein the

immutable memory contains a private key for encrypting the user and security

mechanism identification information **(Sherer, column 7, lines 1-67)**.

Regarding claim 4, the combination of Sherer and Jones teaches wherein the

immutable memory comprises a Read-only Memory (ROM) **(Sherer, fig 3, column 5)**.

Regarding claim 5, the combination of Sherer and Jones does not expressly

disclose wherein the immutable memory further includes a Write-once ROM. However,

Sherer teaches using memory on his device. Therefore, it would have been obvious to

one having ordinary skill in the art at the time the invention was made to use other types

of memory with the system of Sherer. One of ordinary skill in the art would have been

motivated to perform such a modification to provide means for manufacturer to add a

unique identification to the device. Furthermore, this feature has been admitted by

applicant to have been conventional and well known at the time the invention was

made.

Regarding claim 6, the combination of Sherer and Jones teaches wherein the

persistent memory comprises at least one of one of a Complementary Metal Oxide

Semiconductor Random Access Memory (CMOSRAM) and a Programmable Read Only

Memory (PROM) **(Sherer, fig 3, column 5)**.

Regarding claim 7, the combination of Sherer and Jones teaches wherein the

volatile memory comprises a random access memory **(Sherer, fig 3, column 5)**.

Regarding claim 8, the combination of Sherer and Jones teaches wherein the

tamper evident enclosure readily exhibits any attempt to gain access there through to

the memory elements enclosed therein **(column 2, lines 1-67, column 3, lines 1-67,

column 5, lines 1-67, column 6, lines 1-67)**.

Regarding claim 9, the combination of Sherer and Jones teaches wherein the

physical security of the security mechanism depends on the degree of tamper

resistance of the enclosure **(column 2, lines 1-67, column 3, lines 1-67)**.

Conclusion

9.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure. Neuman et al. (US Patent Application Publication 2002/0162026)

teaches an apparatus for providing secure network communication. Wang et al. (US

Patent 6,760,781) teaches a secure network card. Signal's NPL "Cyberguardian Keeps

Hackers, Insider Threats at Bay" and 3Com's NPL "EtherLink 10/100 PCI Network

Interface Card with 3XP processor User Guide" teach the claimed features.

10.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to David G. Cervetti whose telephone number is (571) 272-

5861. The examiner can normally be reached on Monday-Friday 7:00 am - 5:00 pm, off

on Wednesday.

11.   If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Nasser G. Moazzami can be reached on (571) 272-4195. The fax phone

number for the organization where this application or proceeding is assigned is 571-

273-8300.

12.   Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DGC

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1/16/07